Logic gate:

- Block of hardware's, on getting input they produce output 0 or 1.
- Input for logic gates are either 0 or 1.
- Output for logic gates are either 0 or 1.
- Each logic gate has its symbol.
- Operations of logic gate are represented by algebraic expressions.

Names of logic gates:

1. AND logic gate
2. OR logic gate
3. NOT logic gate
4. XOR logic gate
5. NAND logic gate
6. NOR logic gate
7. XNOR logic gate

Logic gate operations:

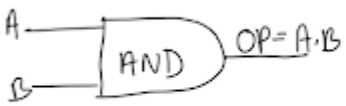
Input variables : A, B Output variable : OP

1. AND : OP = A.B
2. OR : OP = A+B
3. NOT : OP = A'
4. XOR : Exclusive OR : OP = A'B+AB' = A B
5. NAND : NOT AND : OP = (AB)'
6. NOR : NOT OR : OP = (A+B)'

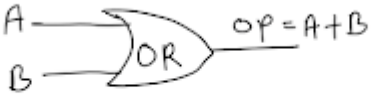
7. XNOR : Exclusive NOR : OP = A'B'+AB = (A B)'

Logic gate symbols:

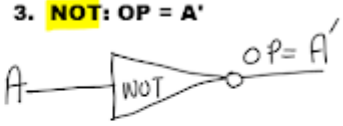
1. **AND : OP = A.B**



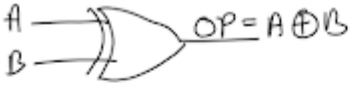
2. **OR : OP = A+B**



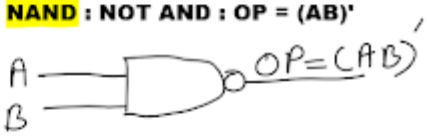
3. **NOT: OP = A'**



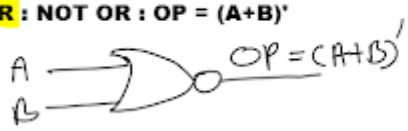
4. **XOR : Exclusive OR : OP = A'B+AB' = A ⊕ B**



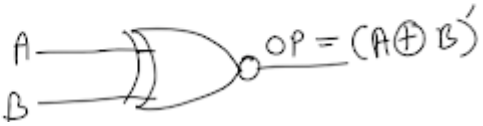
5. **NAND : NOT AND : OP = (AB)'**



6. **NOR : NOT OR : OP = (A+B)'**



7. **XNOR : Exclusive NOR : OP = A'B'+AB = (A ⊕ B)'**

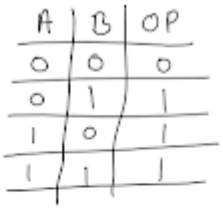


Truth Table:

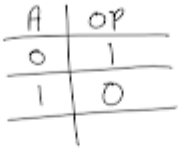
Table shows relationship between input and output variables in logic gates.

1. **AND** : OP = A.B

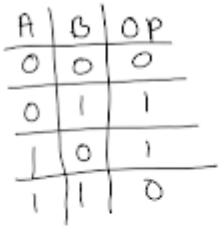
2. **OR** : OP = A+B



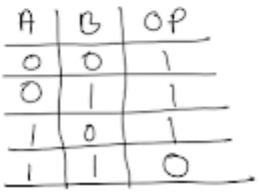
3. **NOT**: OP = A'



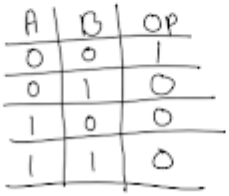
4. **XOR** : Exclusive OR : OP = A'B+AB' = A⊕B



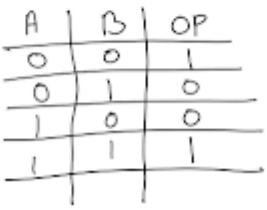
5. **NAND** : NOT AND : OP = (AB)'



6. **NOR** : NOT OR : OP = (A+B)'



7. **XNOR** : Exclusive NOR : OP = A'B'+AB = (A⊕B)'



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34. Differentiate between Serial and parallel data transfer ?
35. Explain signed magnitude, signed l’s complement and signed 2’s complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
36. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?

38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
42. Explain SIMD array processor along with its architectural diagram ?
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44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn’s taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
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