- 1. What is the primary purpose of pipelining in computer architecture?
- A) To increase clock frequency
- B) To decrease instruction latency
- C) To reduce power consumption
- D) To simplify instruction set architecture

Answer: B) To decrease instruction latency

Explanation: Pipelining allows multiple instructions to be processed simultaneously, reducing the time it takes to execute each instruction.

- 2. Which of the following cache mapping techniques provides the fastest access to data?
- A) Direct mapping
- B) Fully associative mapping
- C) Set-associative mapping
- D) Multi-level mapping

View answer

Answer: B) Fully associative mapping

Explanation: In fully associative mapping, any block of main memory can be placed in any cache line, providing the fastest access but requiring more complex hardware.

- 3. What is the purpose of branch prediction in computer architecture?
- A) To eliminate branches in the code

B) To predict the outcome of branch instructions

C) To optimize the execution of floating-point operations

D) To increase the size of the instruction cache

View answer

Answer: B) To predict the outcome of branch instructions

Explanation: Branch prediction attempts to guess whether a conditional branch will be taken or not, allowing the processor to speculatively execute instructions.

4. Which of the following is NOT a characteristic of superscalar processors?

A) Ability to execute multiple instructions simultaneously

B) Dependency checking between instructions

C) Dynamic scheduling of instructions

D) Single-issue pipeline

View answer

Answer: D) Single-issue pipeline

Explanation: Superscalar processors have multiple execution units and can execute multiple instructions per clock cycle, which distinguishes them from single-issue pipelines.

5. What is the purpose of register renaming in out-of-order execution processors?

A) To increase the number of general-purpose registers

B) To map architectural registers to physical registers

- C) To reduce the number of pipeline stages
- D) To simplify the instruction set architecture

Answer: B) To map architectural registers to physical registers

Explanation: Register renaming allows the processor to assign physical registers dynamically, avoiding data hazards and improving performance in out-of-order execution.

- 6. Which of the following memory consistency models provides the strongest ordering guarantees?
- A) Sequential consistency
- B) Weak consistency
- C) Release consistency
- D) Total store ordering

View answer

Answer: A) Sequential consistency

Explanation: Sequential consistency guarantees that the result of any execution is the same as if the operations of all processors were executed in some sequential order.

- 7. Which of the following cache coherence protocols uses a directory-based approach?
- A) MSI (Modified, Shared, Invalid)
- B) MESI (Modified, Exclusive, Shared, Invalid)

- C) MOESI (Modified, Owned, Exclusive, Shared, Invalid)
- D) MESIF (Modified, Exclusive, Shared, Invalid, Forward)

Answer: C) MOESI (Modified, Owned, Exclusive, Shared, Invalid)

Explanation: MOESI protocol is a directory-based cache coherence protocol used to maintain coherence in multiprocessor systems.

- 8. Which of the following is a characteristic of a dataflow architecture?
- A) Execution is driven by the availability of data
- B) Execution is controlled by program counters
- C) Instructions are executed sequentially
- D) Instructions are executed based on branch predictions

View answer

Answer: A) Execution is driven by the availability of data

Explanation: In dataflow architectures, instructions are executed as soon as their operands are available, allowing for parallelism based on data dependencies.

- 9. Which of the following is NOT a feature of vector processors?
- A) Ability to process multiple data elements simultaneously
- B) Hardware support for SIMD operations
- C) Use of vector registers to hold data elements

D) Support for out-of-order execution

View answer

Answer: D) Support for out-of-order execution

Explanation: Vector processors typically execute instructions in order, exploiting parallelism within vector instructions.

- 10. What is the purpose of speculative execution in computer architecture?
- A) To improve branch prediction accuracy
- B) To reduce the overhead of cache coherence protocols
- C) To predict the outcome of memory operations
- D) To execute instructions before it is certain they should be executed

View answer

Answer: D) To execute instructions before it is certain they should be executed

Explanation: Speculative execution allows the processor to execute instructions ahead of time based on branch prediction, improving performance by overlapping computation and memory access.

- 11. Which of the following techniques is used to reduce the impact of memory latency in modern processors?
- A) Cache prefetching
- B) Branch prediction
- C) Register renaming

## D) Scoreboarding

View answer

Answer: A) Cache prefetching

Explanation: Cache prefetching anticipates future memory accesses and fetches data into the cache before it is explicitly requested, reducing the impact of memory latency.

- 12. What is the purpose of a branch target buffer (BTB) in computer architecture?
- A) To store the target addresses of branch instructions
- B) To predict the direction of branch instructions
- C) To buffer the instructions following a taken branch
- D) To manage the allocation of branch predictor resources

View answer

Answer: A) To store the target addresses of branch instructions

Explanation: A BTB caches the target addresses of previously encountered branch instructions, allowing for fast retrieval of branch targets.

- 13. Which of the following is NOT a characteristic of a RISC (Reduced Instruction Set Computing) architecture?
- A) Fixed-length instruction encoding
- B) Large number of addressing modes
- C) Simple and orthogonal instruction set
- D) Load/store architecture

Answer: B) Large number of addressing modes

Explanation: RISC architectures typically have a limited number of addressing modes to simplify instruction decoding and execution.

- 14. What is the purpose of a TLB (Translation Lookaside Buffer) in a computer system?
- A) To cache virtual-to-physical address translations
- B) To store instruction opcodes for quick access
- C) To buffer data during memory transfers
- D) To maintain coherence between cache levels

View answer

Answer: A) To cache virtual-to-physical address translations

Explanation: The TLB caches frequently used translations from virtual memory addresses to physical memory addresses, improving memory access performance.

- 15. Which of the following is a characteristic of SIMD (Single Instruction, Multiple Data) architectures?
- A) Instructions operate on multiple data elements simultaneously
- B) Instructions are executed sequentially
- C) Each instruction can access a different memory location
- D) Instructions are executed out of order

Answer: A) Instructions operate on multiple data elements simultaneously

Explanation: SIMD architectures execute a single instruction on multiple data elements in parallel, exploiting data-level parallelism.

- 16. Which of the following cache replacement policies is based on the principle of "least recently used"?
- A) Random replacement
- B) FIFO (First-In, First-Out) replacement
- C) LRU (Least Recently Used) replacement
- D) LFU (Least Frequently Used) replacement

View answer

Answer: C) LRU (Least Recently Used) replacement

Explanation: LRU replacement evicts the cache line that has not been accessed for the longest time.

- 17. What is the primary advantage of a multi-core processor over a single-core processor?
- A) Higher clock frequency
- B) Greater cache capacity
- C) Increased parallelism
- D) Improved branch prediction accuracy

Answer: C) Increased parallelism

Explanation: Multi-core processors have multiple processing units, allowing them to execute multiple tasks simultaneously and thus increasing overall system throughput.

- 18. Which of the following is NOT a characteristic of VLIW (Very Long Instruction Word) architectures?
- A) Fixed-length instruction encoding
- B) Multiple instructions executed in parallel
- C) Compiler-driven instruction scheduling
- D) Dynamic instruction reordering

View answer

Answer: D) Dynamic instruction reordering

Explanation: VLIW architectures rely on the compiler to schedule instructions for parallel execution, rather than dynamically reordering instructions at runtime.

- 19. Which of the following cache coherence protocols is commonly used in shared-memory multiprocessor systems?
- A) MESI (Modified, Exclusive, Shared, Invalid)
- B) MOESI (Modified, Owned, Exclusive, Shared, Invalid)
- C) MSI (Modified, Shared, Invalid)
- D) MESIF (Modified, Exclusive, Shared, Invalid, Forward)

Answer: A) MESI (Modified, Exclusive, Shared, Invalid)

Explanation: MESI protocol is widely used to maintain cache coherence in shared-memory multiprocessor systems.

- 20. What is the primary advantage of a Non-Uniform Memory Access (NUMA) architecture?
- A) Lower memory latency
- B) Greater memory bandwidth
- C) Simpler cache coherence protocols
- D) Reduced power consumption

View answer

Answer: A) Lower memory latency

Explanation: NUMA architectures reduce memory latency by providing each processor with access to its own local memory, minimizing the need to access remote memory.