Array can be seen as collection of variables.

An variable is declared as :

a DB 2
b DB 3
c DB 4

Here, a, b and c are variable names. And 2, 3, 4 are values assigned to them.

An array is declaed as:

d DB 2, 3, 4

Array eg. 01: Use of DUP operator

a DB 2,2,2,2,2,2,2,2,2

Using DUP operator,

a DB 9 DUP(2)

Array eg. 02: Use of DUP operator

a DB 1,2,3,1,2,3,1,2,3

Using DUP operator:

a DB 3 DUP (1,2,3)

Array Index Number

For example,

a DB 1,2,3,4,5,6

ArrayName[Index Number] = Value
a[0] = 1
a[1] = 2
a[2] = 3
a[3] = 4
a[4] = 5
a[5] = 6

Related posts:

1. Structure of Desktop computers
2. Logic Gates
3. Register Organization
4. Bus structure in Computer Organization
5. Addressing modes

6. Register Transfer Language
7. Numerical problem on Direct mapping
8. Registers in Assembly Language Programming
9. Net 31
10. How to start with GNU Simulator 8085
11. Cache Updating Scheme
12. Cache Memory
13. Principle of Cache Memory
14. Cache Mapping
15. Addition and subtraction in fixed point numbers
16. PCI Bus
17. Booths Algorithm
18. Write a short note on design of arithmetic unit ?
19. Write a short note on Array processors ?
20. Write a short note on LRU algorithm ?
21. What is the format of Micro Instruction in Computer Architecture explain ?
22. What is the layout of pipelined instruction in Computer Architecture ?
23. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
24. What is Memory Organization ? Discuss different types of Memory Organization in Computer System.
25. Computer Organization Q and A
26. Write short note on improving cache performance methods in detail ?
27. What is Multiprocessor ? Explain inter process communication in detail ?
28. Briefly explain the concept of pipelining in detail ?
29. Discuss the following in detail: RISC architecture, Vector processing ?
30. Define the instruction format ? Explain I/O System in detail ?
31. Explain the design of arithmetic and logic unit by taking on example ?

32. Explain how addition and subtraction are performed in fixed point number ?
33. Explain different modes of data transfer between the central computer and I/O device ?
34. Differentiate between Serial and parallel data transfer ?
35. Explain signed magnitude, signed l's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
36. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
42. Explain SIMD array processor along with its architectural diagram ?
43. Write short notes on
44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn's taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?

52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
56. Computer Organization Previous Years Solved Questions
57. Booths algorithm to muliyiply +5 and -15