Two copies of the same data can exist in a cache system at the same time, one in cache and the other in main memory.

The problem is, If one copy is changed while the other remains unchanged, two sets of data are linked with the same address.

In order to prevent this the cache system has updating scheme:

1. Write through system
2. Buffered write through system
3. Write back system

1. Write through system

Data is copied to memory by the cache controller as soon as it is written to the cache. It requires time to write data in main memory with increase in bus traffic. This has the effect of lowering system performance.

2. Buffered write through system

Before the write cycle to the main memory is completed, the CPU can start a new cycle. This indicates that writes to the main memory are buffered.

When main memory is updated in such systems, read access, often known as a “cache hit,” can be conducted simultaneously. However, the processor must wait for consecutive write operations to the main memory or read operations with “cache miss.”

3. Write back system

During the write operation, only the cache location is updated in this approach. The location is then marked with a flag, and the word is copied into main memory when it is removed from the cache.