1. What does CMOS stand for in VLSI circuit design?

a) Complete Metal Oxide Semiconductor
b) Complementary Metal Oxide Semiconductor
c) Centralized Metal Oxide Semiconductor
d) Complex Metal Oxide Semiconductor

Answer: b) Complementary Metal Oxide Semiconductor

In CMOS VLSI circuit design, complementary MOS (Metal Oxide Semiconductor) technology is utilized, where both PMOS (P-channel MOS) and NMOS (N-channel MOS) transistors are employed to achieve low power consumption and high noise immunity.

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2. Which of the following is NOT a step in the VLSI design flow?

a) RTL Design
b) Packaging
c) Physical Design
d) Verification

Answer: b) Packaging

The VLSI design flow typically includes steps such as RTL (Register Transfer Level) design, synthesis, physical design, verification, and testing. Packaging, while crucial for the final product, is not typically considered a part of the VLSI design flow.

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3. Which design strategy emphasizes breaking down complex systems into smaller, more manageable components?

a) Regularity
b) Modularity
c) Locality
d) Hierarchy

Answer: d) Hierarchy

In VLSI design, hierarchy involves organizing the design into multiple levels of abstraction, allowing for easier management and understanding of complex systems.

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4. What is the primary advantage of using MOS transistors as switches in CMOS logic?

a) High power consumption
b) Low noise immunity
c) Low static power consumption
d) Low speed

Answer: c) Low static power consumption

MOS transistors used in CMOS logic circuits offer low static power consumption due to their ability to maintain either a high or low output state without consuming significant power, making them ideal as switches in digital circuits.

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5. Which type of logic circuit performs a specific Boolean function based on the input values at that instant?

a) Sequential circuit
b) Combinational circuit
c) Latch
d) Register

Answer: b) Combinational circuit

Combinational circuits produce outputs solely based on the current input values without considering previous input or output states.

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6. Which CAD tool stage involves converting a high-level design description into a gate-level netlist?

a) Design entry
b) Synthesis

c) Functional simulation
d) Layout

Answer: b) Synthesis

Synthesis is the process of translating a high-level design description, often in a hardware description language (HDL), into a gate-level netlist that represents the logical structure of the circuit.

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7. Which characteristic of design emphasizes the repetitive use of standard cells to simplify layout and manufacturing?

a) Regularity
b) Modularity
c) Locality
d) Hierarchy

Answer: a) Regularity

Regularity in design refers to the consistent and repetitive use of standard cells, which simplifies layout and manufacturing processes, leading to more predictable and efficient designs.

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8. Which CAD tool stage involves verifying the functionality of the design using test vectors?

a) Design entry
b) Synthesis
c) Functional simulation
d) Layout

Answer: c) Functional simulation

Functional simulation involves testing the functionality of the design by applying various input vectors and verifying that the output matches the expected behavior.

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9. Which type of circuit storage element retains its state indefinitely until explicitly changed?

a) Combinational circuit
b) Latch
c) Register
d) Sequential circuit

Answer: b) Latch

Latches are sequential logic elements that store data indefinitely until new data is provided

to change their state.

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10. What is the primary goal of the design entry stage in CAD tool flow?

a) Translating a gate-level netlist into physical layout
b) Verifying the functionality of the design
c) Creating a high-level description of the desired circuit behavior
d) Optimizing the design for area and power

Answer: c) Creating a high-level description of the desired circuit behavior

The design entry stage involves creating a high-level description of the desired circuit behavior, often using a hardware description language (HDL) or graphical schematic entry tools. This description serves as the basis for subsequent design and verification stages.