- 1. What is the format of Micro Instruction in Computer Architecture explain?
- 2. Write a short note on LRU algorithm?
- 3. Write a short note on Array processors?
- 4. Write a short note on design of arithmetic unit?
- 5. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
- 6. What is the layout of pipelined instruction in Computer Architecture?
- 7. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
- 8. What is Memory Organization ? Discuss different types of Memory Organization in Computer System.
- 9. Briefly explain the concept of pipelining in detail?
- 10. What is Multiprocessor? Explain inter process communication in detail?
- 11. Write short note on improving cache performance methods in detail?
- 12. Briefly explain the concept of pipelining in detail?
- 13. What is Multiprocessor? Explain inter process communication in detail?
- 14. Explain different modes of data transfer between the central computer and I/O device ?
- 15. Explain how addition and subtraction are performed in fixed point number?
- 16. Explain the design of arithmetic and logic unit by taking on example?
- 17. Define the instruction format? Explain I/O System in detail?
- 18. Discuss the following in detail: RISC architecture, Vector processing?
- 19. Explain how a stack organized computer executes instructions? What is Stack?
- 20. Explain hardwired microprogrammed control unit? What is address sequencer circuit?
- 21. If cache access time is IOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
- 22. Explain signed magnitude, signed I's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.

- 23. Differentiate between Serial and parallel data transfer?
- 24. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
- 25. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
- 26. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
- 27. Explain general register organization.
- 28. Draw the functional and structural views of a computer system and explain in detail?
- 29. Write short notes on
- 30. Explain SIMD array processor along with its architectural diagram?
- 31. Explain the various pipeline vector processing methods?
- 32. Define the following: a) Flynn's taxonomy b) Replacement algorithm
- 33. Compare and contrast DMA and I/O processors?
- 34. Explain arithmetic pipeline?
- 35. What is mapping? Name all the types of cache mapping and explain anyone in detail.
- 36. Explain arithmetic pipeline?
- 37. What is mapping? Name all the types of cache mapping and explain anyone in detail.
- 38. Explain any page replacement algorithm with the help of example?
- 39. What are different addressing modes? Explain them.
- 40. Describe the language features for parallelism?
- 41. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
- 42. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
- 43. Describe the subroutine. Write a program which move the block of data. Write a note on subroutines.
- 44. Discuss the advantages and disadvantages of synchronous and asynchronous

transmission.

- 45. Explain synchronous communication and asynchronous communication.
- 46. What do you mean by serial communication? What are the transmission modes of serial communication?
- 47. Explain I/O channels with its types.
- 48. What do you mean by Input-Output (I/O) processor?
- 49. What is the difference between isolated I/O and memory mapped I/O? Explain the advantages and disadvantages of each.
- 50. Write short note on DMA. OR Explain the working of DMA controller with the help of suitable diagrams. OR Write a short note on DMA based data transfer. OR Give the block diagram of DMA controller. Why are the read andwrite control lines in a DMA controller bidirectional?
- 51. What is interrupt initiated I/O?
- 52. Write a short note on programmed I/O. OR Discuss the programmed I/O method for controlling input-output operations.
- 53. Explain the types of interrupt on the basis of timer.
- 54. Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.
- 55. How interrupts are classified?
- 56. How system resolve the priority of interrupt ?OR Explain polling and daisy chaining method.
- 57. Explain the sequence that takes place when an interrupt occurs.
- 58. Write a short note on interrupts. OR Define interrupt. When a device interrupt occurs how does the processor determine which device has issued the interrupt?
- 59. Explain I/O bus and I/O command.
- 60. Describe I/O interface. Why they are needed ?OR Why input-output interface is required ? Describe in detail.

- 61. Explain the term peripheral devices.
- 62. What do you mean by locality of reference? Explain with suitable example.
- 63. Discuss the conceptual organization of a multilevel memory system used in computers.
- 64. What do you mean by CAM? Explain its major characteristics.
- 65. Explain the following memory schemes discussing why needed the : i. Interleaved memory ii. Associative memory Explain the working principle of associative memory.
- 66. What is virtual memory ?OR Write a short note on virtual memory.
- 67. A moving arm disc storage device has the following specifications: Number of Tracks per recording surface = 200 Disc rotation speed = 2400 revolution/minute Track-storage capacity = 62500 bits /Estimate the average latency and data transfer rate of this device.
- 68. Explain auxiliary memory. What are the commonly used auxiliary memory?
- 69. Explain replacement algorithm in brief.
- 70. Write short note on write through and write back policy of cache memory.
- 71. What is the distinction between spatial locality and temporal locality?
- 72. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128 K \times 32. i. Formulate all pertinent information required to construct the cache memory.ii. What is the size of the cache memory?
- 73. What do you mean by cache memory? How does itaffect the performance of the computer system? An eight-way set associative cache is used in computer in which the real memory size 232 bytes. The line size is 16 bytes, and there are 210 lines per set. Calculate the cache size and tag length.
- 74. Consider a cache uses a direct mapping scheme. The size of main memory is 4 K bytes and word size of cache is 2 bytes. The size of cache memory is 128 bytes. Find the following: i. The size of main memory address (assume each byte of main memory has

- an address) ii. Address of cache block iii. How many memory location address will be translated to cache address/block/location? iv. How can it be determined if the content of specified main memory address in cache?
- 75. What is meant by cache mapping? What are different types of mapping? Discuss different mapping techniques with examples.ORDiscuss the various types of address mapping used in cache memory.
- 76. How the performance of cache memory is measured?
- 77. Discuss the design issues in cache design.
- 78. Write short note on cache memory.
- 79. A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specific one of 64 register and an address part. i. How many bits are there in the operation code, the register code part and the address part? ii. Draw the instruction word format and indicate the number of bits in each part. iii. How many bits are there in the data and address inputs of the memory?
- 80. A ROM chip of 1024*8 has four select inputs and operates from a 5 volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.
- 81. A computer uses RAM chips of 1024*1 capacity. i. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024*8? ii. How many chips are needed to provide a memory capacity of 16 KB? Explain in words how the chips are to be connected to the address bus.
- 82. How main memory is useful in computer system ?Explain the memory address map of RAM and ROM.
- 83. What is ROM? Explain the types of ROM.OR Explain the semi conductor based ROM memories.
- 84. Explain 2D, 2 12 D memory organization. Memory OR Write short note on organization

- of 2D and 2.5D memory organization.
- 85. Give the structure of commercial $8M \times 8$ bit DRAM chip
- 86. Explain semiconductor RAM. Enlist the types of semiconductor memory.OR Explain dynamic RAM and static RAM.
- 87. Explain concept of memory. Describe memory hierarchy
- 88. Write a program loop using a pointer and a counter toclear the contents of hex locations 500 to 5FF with 0.
- 89. Explain 4-bit incrementer with a necessary diagram.
- 90. Write an assembly level program for the following pseudo code : SUM = 0 SUM = SUM + A + B DIF = DIF-C SUM = SUM + DIF
- 91. Briefly define the following terms : i. Micro-operation ii. Micro-instruction iii. Micro-program iv. Micro-code v. Control memory
- 92. Explain the concept of vertical and horizontal multi-programming
- 93. Describe micro-program sequencing in detail.
- 94. Explain micro-program sequencer for a control memory using asuitable block diagram. OR What is a micro-program sequencer? With block diagram, explainthe working of micro-program sequencer.
- 95. Discuss the basic structure of micro-program control unit.OR Explain micro-programmed control unit.
- 96. Explain hardwired control unit. What are the methods to design hardwired controllers?

 OR What do you understand by hardwired control? Give various methods to design hardwired control unit. Describe any one method used for designing of hardwired control unit.
- 97. Differentiate between linear and non-linear pipeline.
- 98. How pipelining is classified ?OR Write short notes on instruction pipeline.
- 99. What is pipelining? How the idea of pipelining used ina computer ?OR Write a short note on pipelining.

- 100. Differentiate between RISC & CISC based microprocessor. OR Differentiate between complex instruction set computer and reduced instruction set computer.
- 101. Write a short note on RISC. OR What is RISC? Explain its various characteristics.
- 102. Discuss the advantages and disadvantages of using avariable length instruction format.
- 103. What is CISC? Explain its characteristics.
- 104. Discuss the execution of a complete instruction.
- 105. Write a short note on shift micro-operations.OR List and explain different types of shift micro-operation.
- 106. Write short note on arithmetic micro-operation.
- 107. Write a short note on register transfer micro-operation.
- 108. Describe micro-operation and enlist its types.
- 109. In an instruction format, there are 16 bits in an instruction word. Bit 0 to 11 convey the address of the memory location for memory related instructions. For non memory instructions these bits convey various register or I/O operations. Bits 12 to 14 show the various basic memory operations such asADD, AND, LDA etc. Bit 15 shows if the memory is accessed directly or indirectly. For such an instruction format draw block diagram of the control unit of a computer and briefly explain how an instruction will be decoded and executed, by this control unit.
- 110. Assuming that all registers initially contain 0, what is the value of R1after the following instruction sequence is executed: MOV R1, # 6 MOV R2, # 5 ADD R3, R1, R1 SUB R1, R3, R2 MUL R3, R1, R1.
- 111. Write the steps in fetching a word from memory. Differentiate between a branch instruction and call sub routine instruction.
- 112. Define instruction cycle and divide instruction cycle into sub cycles with the help of diagram, explain the sequence in which sub cycles are executed.OR Explain the different cycles of an instruction execution.OR Explain all the phases of instruction

cycle.

- 113. Evaluate the arithmetic statement X = (A + B)*(C + D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression.
- 114. Describe the types of instructions on the basis of address fields used in the instruction with example.
- 115. Describe the types of instructions on the basis of address fields used in the instruction with example.
- 116. What is an instruction in the context of computer organization? Explain the purpose of the various elements of an instruction with the help of a sample instruction format.
- 117. Represent 1460. 125 base 10 in single precision and double precision formats.
- 118. Explain IEEE standard for floating point numbers.OR How floating point numbers are represented in computer, also give IEEE 754 standard 32-bit floating point number format.
- 119. Draw a flow chart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.
- 120. Draw the block diagram of control unit of basic computer. Explain in detail with control timing diagrams.
- 121. Add 35 and 31 in binary using 8-bit registers, in signed1's complement and signed 2's complement.
- 122. Explain the function of arithmetic circuit with the help of circuit diagram.
- 123. Write the steps for various floating point arithmetic operations.
- 124. Explain the basic format used to represent floating point numbers.
- 125. Perform the division process of 00001111 by 0011 (use adividend of 8 bits).
- 126. Draw the data path of sequential n-bit binary divider. Give the non-restoring division algorithm for unsigned integers. Also illustrate algorithm for unsigned integer with a suitable example.

- 127. What do you mean by over flow? Describe the over flow detection.
- 128. Draw the flow chart for restoring and non-restoring division operation.
- 129. Write down the step for restoring and non-restoring of division operations.
- 130. Explain array multiplier method with the help of example.
- 131. Draw the data path of 2's compliment multiplier. Give the Robertson multiplication algorithm for 2's compliment fractions. Also illustrate the algorithm for 2's compliment fraction by a suitable example.
- 132. Show the multiplication process using Booth's algorithm when the following numbers are multiplied: (-13) by (+8).
- 133. Show the contents of the registers E, A, Q, SC during theprocess of multiplication of two binary numbers 11111 (multiplicand) 10101 (multiplier). The signs are not included.
- 134. Show step by step the multiplication process using Booth's algorithm when (+ 15) and (- 13) numbers are multiplied. Assume 5-bit registers that hold signed numbers.
- 135. Explain Booth's algorithm with its hardware implementation.
- 136. Explain the Booth's algorithm in depth with the help off low chart. Give an example for multiplication using Booth's algorithm. OR Discuss the Booth's algorithm for 2's complement number. Also illustrate it with the some example.OR Explain Booth's multiplication algorithm in detail.
- 137. Write short note on look ahead carry adders.
- 138. Describe sequential Arithmetic and Logic Unit (ALU)using proper diagram.
- 139. How addressing mode is significant for referring memory? List and explain different types of addressing modes.
- 140. Describe auto increment and auto decrement addressing modes with proper example
- 141. What is difference between implied and immediate addressing modes? Explain with an example.

- 142. Write short note on relative addressing mode and indirect addressing mode. OR

 Explain the following addressing modes with the help of an example each :i. Direct ii.

 Register indirect iii. Implied iv. Immediate v. Indexed
- 143. Explain an accumulator based central processing unit organization with block diagram.
- 144. What is the stack organization? Compare register stackand memory stack.
- 145. What is a memory stack? Explain its role in managing subroutines with the help of neat diagrams.
- 146. What is stack? Give the organization of register stack with all necessary elements and explain the working of push and pop operations.
- 147. Explain general-purpose register based organization.
- 148. What is the benefit of using multiple bus architecture compared to a single bus architecture?
- 149. Explain why the single shared bus is so widely used asan inter connection medium in both sequential and parallel computers. What are its main disadvantages?
- 150. Explain the operation of three state bus buffers and show its use in design of common bus.
- 151. What is memory transfer? What are different registers associated for memory transfer? Discuss.
- 152. Discuss the advantages and disadvantages of pollingand daisy chaining bus arbitration schemes.OR Explain daisy changing method. Write its advantages and disadvantages.
- 153. Discuss the bus arbitration. OR Write a short note on bus arbitration.
- 154. Describe the architecture of bus.
- 155. What is a bus in digital system? Also explain its types.
- 156. Explain the functional units of digital system and their inter connections.
- 157. Draw a block diagram of a computer's CPU showing all the basic building blocks such as program counter, accumulator, address and data registers, instruction register, control unit etc., and describe how such an arrangement can work as a computer,

ifconnected properly to memory, input/output etc.

Related posts:

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- 16. Cache Mapping
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