Maskable and non-maskable interrupt

Maskable and non-maskable interrupt are two types of interrupts that a computer processor can receive.

Maskable interrupts can be disabled or enabled by the programmer through the use of a mask or flag. When a maskable interrupt occurs, the processor checks the interrupt mask to determine if the interrupt should be serviced or ignored. Examples of maskable interrupts include I/O interrupts and software interrupts.

Non-maskable interrupts, on the other hand, cannot be disabled or ignored by the programmer. They are typically reserved for critical system events such as power failure or hardware errors, which require immediate attention from the processor. When a non-maskable interrupt occurs, the processor interrupts the current operation and immediately services the interrupt.

RISC and CISC

RISC and CISC are two different computer processor architectures.

RISC stands for Reduced Instruction Set Computing. In a RISC architecture, the instruction set is simplified, and the processor executes a large number of simple instructions. RISC architectures typically have a small number of general-purpose registers and rely on software optimization to achieve high performance. Examples of RISC architectures include ARM and MIPS.

CISC stands for Complex Instruction Set Computing. In a CISC architecture, the instruction set is more complex, and the processor can execute complex instructions that perform multiple

operations in a single instruction. CISC architectures typically have a larger number of specialized registers and rely on hardware optimization to achieve high performance. Examples of CISC architectures include x86 and x64.

In general, RISC architectures are considered to be more efficient and easier to program, while CISC architectures are more flexible and better suited for complex applications.

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