Cache design involves several critical considerations to optimize performance and cost-effectiveness. The primary elements influencing cache design include:

i. Cache Size:

a. Small Size: To keep costs close to main memory.

b. Large Size: To maximize the chances of having most memory references in the cache, reducing average access time.

ii. Block Size:

a. Importance: Influences cache performance significantly.

b. Larger Block Size: Increases hit ratio as more data, including adjacent words, can be stored.

c. Small Block Size: Results in frequent replacement, increasing overhead in cache operation.

d. Hit Ratio vs. Block Size: Initially, increasing block size improves hit ratio, but it may decrease after a certain point.

iii. Associativity:

- Tradeoff: Balancing parallel searching against constraints on which addresses can be stored.
- Higher Associativity: Allows for more flexible storage but may increase complexity and cost.

iv. Write Strategy:

- Concern: Determines when cache contents are written to main memory.
- Explanation:
    - Write-Through: Immediately updates main memory with every write operation.
    - Advantage: Ensures consistency between cache and main memory.
    - Disadvantage: Slower due to frequent writes.
    - Write-Back: Delays updating main memory until the cache block is replaced.
    - Advantage: Reduces write operations, improving speed.
    - Disadvantage: Requires additional mechanisms to track changes.

Related posts:

1. Draw a block diagram of a computer’s CPU showing all the basic building blocks such as program counter, accumulator,address and data registers, instruction register, control unit etc.,and describe how such an arrangement can work as a computer, ifconnected properly to memory, input/output etc.
2. Explain the functional units of digital system and their inter connections.
3. What is a bus in digital system ? Also explain its types.
4. Describe the architecture of bus.
5. Discuss the bus arbitration.OR Write a short note on bus arbitration.
6. Discuss the advantages and disadvantages of pollingand daisy chaining bus arbitration schemes.OR Explain daisy changing method. Write its advantages and disadvantages.
7. What is memory transfer ? What are different registers associated for memory transfer ? Discuss.
8. Explain the operation of three state bus buffers and show its use in design of common bus.
9. Explain why the single shared bus is so widely used asan inter connection medium in

both sequential and parallel computers. What are its main disadvantages ?

10. What is the benefit of using multiple bus architecture compared to a single bus architecture ?
11. Explain general-purpose register based organization.
12. What is stack ? Give the organization of register stack with all necessary elements and explain the working of push and pop operations.
13. What is a memory stack ? Explain its role in managing subroutines with the help of neat diagrams.
14. What is the stack organization ? Compare register stackand memory stack.
15. Explain an accumulator based central processing unit organization with block diagram.
16. Write short note on relative addressing mode and indirect addressing mode. OR Explain the following addressing modes with the help of an example each :i. Direct ii. Register indirect iii. Implied iv. Immediate v. Indexed
17. What is difference between implied and immediate addressing modes ? Explain with an example.
18. Describe auto increment and auto decrement addressing modes with proper example ?
19. How addressing mode is significant for referring memory ? List and explain different types of addressing modes.
20. Describe sequential Arithmetic and Logic Unit (ALU)using proper diagram.
21. Write short note on look ahead carry adders.
22. Explain the Booth’s algorithm in depth with the help off low chart. Give an example for multiplication using Booth’s algorithm. OR Discuss the Booth’s algorithm for 2’s complement number. Also illustrate it with the some example.OR Explain Booth’s multiplication algorithm in detail.
23. Explain Booth’s algorithm with its hardware implementation.
24. Show step by step the multiplication process using Booth’s algorithm when (+ 15) and

(– 13) numbers are multiplied.Assume 5-bit registers that hold signed numbers.

25. Show the contents of the registers E, A, Q, SC during theprocess of multiplication of two binary numbers 11111 (multiplicand) 10101 (multiplier). The signs are not included.
26. Show the multiplication process using Booth's algorithm when the following numbers are multiplied : (– 13) by (+ 8).
27. Draw the data path of 2's compliment multiplier. Give the Robertson multiplication algorithm for 2's compliment fractions.Also illustrate the algorithm for 2's compliment fraction by a suitable example.
28. Explain array multiplier method with the help of example.
29. Write down the step for restoring and non-restoring of division operations.
30. Draw the flow chart for restoring and non-restoring division operation.
31. What do you mean by over flow ? Describe the over flow detection.
32. Draw the data path of sequential n-bit binary divider.Give the non-restoring division algorithm for unsigned integers.Also illustrate algorithm for unsigned integer with a suitable example.
33. Perform the division process of 00001111 by 0011 (use adividend of 8 bits).
34. Explain the basic format used to represent floating point numbers.
35. Write the steps for various floating point arithmetic operations.
36. Explain the function of arithmetic circuit with the help of circuit diagram.
37. Add – 35 and – 31 in binary using 8-bit registers, in signed1's complement and signed 2's complement.
38. Draw the block diagram of control unit of basic computer. Explain in detail with control timing diagrams.
39. Draw a flow chart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.
40. Explain IEEE standard for floating point numbers.OR How floating point numbers are

represented in computer, also give IEEE 754 standard 32-bit floating point number format.

41. Represent 1460. 125 base 10 in single precision and double precision formats.
42. What is an instruction in the context of computer organization ? Explain the purpose of the various elements of an instruction with the help of a sample instruction format.
43. Describe the types of instructions on the basis of address fields used in the instruction with example.
44. Describe the types of instructions on the basis of address fields used in the instruction with example.
45. Evaluate the arithmetic statement X = (A + B)*(C + D)using a general register computer with three address, two address and one address instruction format a program to evaluate the expression.
46. Define instruction cycle and divide instruction cycle into sub cycles with the help of diagram, explain the sequence in which sub cycles are executed.OR Explain the different cycles of an instruction execution.OR Explain all the phases of instruction cycle.
47. Write the steps in fetching a word from memory.Differentiate between a branch instruction and call sub routine instruction.
48. Assuming that all registers initially contain 0, what is the value of R1after the following instruction sequence is executed : MOV R1, # 6 MOV R2, # 5 ADD R3, R1, R1 SUB R1, R3, R2 MUL R3, R1, R1.
49. In an instruction format, there are 16 bits in an instruction word. Bit 0 to 11 convey the address of the memory location for memory related instructions. For non memory instructions these bits convey various register or I/O operations. Bits 12 to 14 show the various basic memory operations such asADD, AND, LDA etc. Bit 15 shows if the memory is accessed directly or indirectly. For such an instruction format draw block diagram of the control unit of a computer and briefly explain how an instruction will be

decoded and executed, by this control unit.

50. Describe micro-operation and enlist its types.
51. Write a short note on register transfer micro-operation.
52. Write short note on arithmetic micro-operation.
53. Write a short note on shift micro-operations.OR List and explain different types of shift micro-operation.
54. Discuss the execution of a complete instruction.
55. What is CISC ? Explain its characteristics.
56. Discuss the advantages and disadvantages of using avariable length instruction format.
57. Write a short note on RISC. OR What is RISC ? Explain its various characteristics.
58. Differentiate between RISC & CISC based microprocessor. OR Differentiate between complex instruction set computer and reduced instruction set computer.
59. What is pipelining ? How the idea of pipelining used ina computer ?OR Write a short note on pipelining.
60. How pipelining is classified ?OR Write short notes on instruction pipeline.
61. Differentiate between linear and non-linear pipeline.
62. Explain hardwired control unit. What are the methods to design hardwired controllers ? OR What do you understand by hardwired control ? Give various methods to design hardwired control unit. Describe any one method used for designing of hardwired control unit.
63. Discuss the basic structure of micro-program control unit.OR Explain micro-programmed control unit.
64. Explain micro-program sequencer for a control memory using asuitable block diagram. OR What is a micro-program sequencer ? With block diagram, explainthe working of micro-program sequencer.
65. Describe micro-program sequencing in detail.

66. Explain the concept of vertical and horizontal multi-programming
67. Briefly define the following terms : i. Micro-operation ii. Micro-instruction iii. Micro-program iv. Micro-code v. Control memory
68. Write an assembly level program for the following pseudo code : SUM = 0 SUM = SUM + A + B DIF = DIF-C SUM = SUM + DIF
69. Explain 4-bit incrementer with a necessary diagram.
70. Write a program loop using a pointer and a counter toclear the contents of hex locations 500 to 5FF with 0.
71. Explain concept of memory. Describe memory hierarchy
72. Explain semiconductor RAM. Enlist the types of semiconductor memory.OR Explain dynamic RAM and static RAM.
73. Give the structure of commercial 8M × 8 bit DRAM chip
74. Explain 2D, 2 12 D memory organization. Memory OR Write short note on organization of 2D and 2.5D memory organization.
75. What is ROM ? Explain the types of ROM.OR Explain the semi conductor based ROM memories.
76. How main memory is useful in computer system ?Explain the memory address map of RAM and ROM.
77. A computer uses RAM chips of 1024*1 capacity. i. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024*8 ? ii. How many chips are needed to provide a memory capacity of 16 KB ? Explain in words how the chips are to be connected to the address bus.
78. A ROM chip of 1024*8 has four select inputs and operates from a 5 volt power supply. How many pins are needed for the IC package ? Draw a block diagram and label all input and output terminals in the ROM.
79. A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts : an indirect bit,

an operation code, a register code part to specific one of 64 register and an address part. i. How many bits are there in the operation code, the register code part and the address part ? ii. Draw the instruction word format and indicate the number of bits in each part. iii. How many bits are there in the data and address inputs of the memory ?

80. Write short note on cache memory.
81. How the performance of cache memory is measured ?
82. What is meant by cache mapping ? What are different types of mapping ? Discuss different mapping techniques with examples.ORDiscuss the various types of address mapping used in cache memory.
83. Consider a cache uses a direct mapping scheme. The size of main memory is 4 K bytes and word size of cache is 2 bytes.The size of cache memory is 128 bytes. Find the following : i. The size of main memory address (assume each byte of main memory has an address) ii. Address of cache block iii. How many memory location address will be translated to cache address/block/location ? iv. How can it be determined if the content of specified main memory address in cache ?
84. What do you mean by cache memory ? How does itaffect the performance of the computer system ? An eight-way set associative cache is used in computer in which the real memory size 232 bytes. The line size is 16 bytes, and there are 210 lines per set.Calculate the cache size and tag length.
85. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128 K × 32. i. Formulate all pertinent information required to construct the cache memory.ii. What is the size of the cache memory ?
86. What is the distinction between spatial locality and temporal locality ?
87. Write short note on write through and write back policy of cache memory.
88. Explain replacement algorithm in brief.
89. Explain auxiliary memory. What are the commonly used auxiliary memory ?

90. A moving arm disc storage device has the following specifications : Number of Tracks per recording surface = 200 Disc rotation speed = 2400 revolution/minute Track-storage capacity = 62500 bits /Estimate the average latency and data transfer rate of this device.
91. What is virtual memory ?OR Write a short note on virtual memory.
92. . Explain the following memory schemes discussing why needed the : i. Interleaved memory ii. Associative memory Explain the working principle of associative memory.
93. What do you mean by CAM ? Explain its major characteristics.
94. Discuss the conceptual organization of a multilevel memory system used in computers.
95. What do you mean by locality of reference ? Explain with suitable example.
96. Explain the term peripheral devices.
97. Describe I/O interface. Why they are needed ?OR Why input-output interface is required ? Describe in detail.
98. Explain I/O bus and I/O command.
99. Write a short note on interrupts. OR Define interrupt. When a device interrupt occurs how does the processor determine which device has issued the interrupt ?
100. Explain the sequence that takes place when an interrupt occurs.
101. How system resolve the priority of interrupt ?OR Explain polling and daisy chaining method.
102. How interrupts are classified ?
103. Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.
104. Explain the types of interrupt on the basis of timer.
105. Write a short note on programmed I/O. OR Discuss the programmed I/O method for controlling input-output operations.
106. What is interrupt initiated I/O ?

107. Write short note on DMA. OR Explain the working of DMA controller with the help of suitable diagrams. OR Write a short note on DMA based data transfer. OR Give the block diagram of DMA controller. Why are the read andwrite control lines in a DMA controller bidirectional ?
108. What is the difference between isolated I/O and memory mapped I/O ? Explain the advantages and disadvantages of each.
109. What do you mean by Input-Output (I/O) processor ?
110. Explain I/O channels with its types.
111. What do you mean by serial communication ? What are the transmission modes of serial communication ?
112. Explain synchronous communication and asynchronous communication.
113. Discuss the advantages and disadvantages of synchronous and asynchronous transmission.
114. Describe the subroutine. Write a program which move the block of data. Write a note on subroutines.