RISC Architecture:

Reduced Instruction Set Computing (RISC) is a type of computer architecture that emphasizes the use of a small, highly optimized set of instructions. The design philosophy behind RISC architecture is to simplify the processor design and to make it more efficient by reducing the complexity of instructions.

In RISC architecture, instructions are designed to be simple and fast, typically executing in one clock cycle. The number of instructions in a RISC architecture is typically much smaller than in a Complex Instruction Set Computing (CISC) architecture, which allows for a simpler processor design and faster instruction execution. RISC processors also use a load/store architecture, which means that arithmetic and logical operations are performed on data stored in registers, rather than directly on memory.

The advantages of RISC architecture include faster instruction execution, simpler processor design, and improved power efficiency. However, RISC architecture can have a higher instruction count for some operations, and it may require more memory to store instructions due to the smaller instruction set.

Vector Processing:

Vector processing is a type of computer architecture that emphasizes the use of vector operations, where a single instruction operates on multiple data elements simultaneously. In vector processing, a group of data elements is stored in a single register, and a single instruction is used to operate on all the data elements in the register.

Vector processing is particularly useful for applications that require large amounts of data to be processed in parallel, such as graphics processing, scientific computing, and artificial

intelligence. By using vector operations, vector processing can perform a large number of operations in parallel, which can result in significant performance improvements over traditional scalar processing.

The advantages of vector processing include improved performance, increased throughput, and reduced power consumption. However, vector processing requires specialized hardware, and it may not be suitable for applications that do not require large amounts of parallel processing.

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49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
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