

Explain different modes of data transfer between the central computer and I/O device ?

In a computer system, there are several modes of data transfer between the central processing unit (CPU) and input/output (I/O) devices.

These modes of transfer can be broadly categorized into three types:

1. Programmed I/O
2. Interrupt-driven I/O
3. Direct memory access (DMA).

## 1. Programmed I/O:

In programmed I/O, the CPU directly controls the transfer of data between the I/O device and memory. The CPU sends commands to the I/O device to start a data transfer, and then waits for the transfer to complete before proceeding with other tasks. This method is suitable for small amounts of data transfer where the CPU has enough time to handle the data transfer.

## 2. Interrupt-driven I/O:

In interrupt-driven I/O, the CPU sends a command to the I/O device to start a data transfer and then proceeds with other tasks. When the data transfer is complete, the I/O device generates an interrupt to inform the CPU that the transfer is finished. The CPU then handles the interrupt, retrieves the data, and continues with its normal processing. Interrupt-driven I/O is suitable for handling large amounts of data transfer where the CPU cannot wait for the transfer to complete.

## 3. Direct Memory Access (DMA):

In DMA, a separate DMA controller is used to manage the transfer of data between the I/O

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device and memory, without the involvement of the CPU. The CPU sets up the DMA controller with the necessary information for the data transfer, and the DMA controller takes over the transfer process. The CPU is free to handle other tasks while the DMA controller transfers the data. Once the transfer is complete, the DMA controller sends an interrupt to the CPU to inform it that the transfer is finished. DMA is suitable for handling large amounts of data transfer where the CPU cannot wait for the transfer to complete.

## Advantages and disadvantages.

### Programmed I/O

Programmed I/O is simple and suitable for small data transfer, but it is slow and wastes CPU time.

### Interrupt-driven I/O

Interrupt-driven I/O is suitable for handling larger amounts of data transfer, but it requires more hardware support and introduces overhead due to interrupts.

### DMA

DMA is the fastest method of data transfer but requires dedicated hardware and complex software support.

The choice of data transfer mode depends on the requirements of the system and the nature of the data being transferred.

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35. Explain signed magnitude, signed 1's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
36. If cache access time is 100ns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
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44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?

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47. Define the following: a) Flynn's taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
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57. Booths algorithm to multiply +5 and -15