

If cache access time is 100ns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.

Hit ratio

Hit ratio is a measure of how often a requested data item is found in a cache. It is defined as the ratio of the number of cache hits to the total number of memory access requests.

In this case, the hit ratio is given as 0.9, which means that 90% of memory access requests result in a cache hit. Therefore, the remaining 10% of memory access requests result in a cache miss, which requires accessing the main memory.

The average access time can be calculated as follows:

$$\text{Average Access Time} = \text{Hit Time} + \text{Miss Rate} \times \text{Miss Penalty}$$

where:

Hit Time = time to access data in cache = 100 ns

Miss Rate = $(1 - \text{Hit Ratio}) = 0.1$ (i.e., 10% of memory access requests result in a cache miss)

Miss Penalty = time to access data in main memory = 1000 ns

Plugging in the values, we get:

$$\begin{aligned}\text{Average Access Time} &= 100 \text{ ns} + 0.1 \times 1000 \text{ ns} \\ &= 100 \text{ ns} + 100 \text{ ns} \\ &= 200 \text{ ns}\end{aligned}$$

Therefore, the average access time is 200 ns.

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19. Write a short note on design of arithmetic unit ?
20. Write a short note on Array processors ?
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22. What is the format of Micro Instruction in Computer Architecture explain ?
23. What is the layout of pipelined instruction in Computer Architecture ?
24. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
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28. What is Multiprocessor ? Explain inter process communication in detail ?
29. Briefly explain the concept of pipelining in detail ?
30. Discuss the following in detail: RISC architecture, Vector processing ?
31. Define the instruction format ? Explain I/O System in detail ?
32. Explain the design of arithmetic and logic unit by taking an example ?
33. Explain how addition and subtraction are performed in fixed point number ?
34. Explain different modes of data transfer between the central computer and I/O device ?
35. Differentiate between Serial and parallel data transfer ?
36. Explain signed magnitude, signed 1's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
42. Explain SIMD array processor along with its architectural diagram ?
43. Write short notes on
44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn's taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?

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49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
56. Computer Organization Previous Years Solved Questions
57. Booths algorithm to multiply +5 and -15