1. What is a common performance metric used for modern processors based on cache architecture?

a) Cache Efficiency Ratio
b) Memory Hit Ratio
c) Cache Miss Rate
d) Pipeline Throughput

Answer: c) Cache Miss Rate
Explanation: Cache miss rate indicates the percentage of memory accesses that result in cache misses, which is a crucial performance metric for cache-based architectures. Lower cache miss rates typically lead to better performance.

2. Which principle states that the number of transistors on integrated circuits doubles approximately every two years?

a) Moore's Law
b) Amdahl's Law
c) Gustafson's Law
d) Murphy's Law

Answer: a) Moore's Law
Explanation: Moore's Law, formulated by Gordon Moore, states that the number of transistors on a microchip doubles approximately every two years, leading to rapid advancements in processor performance and capabilities.

3. What is the primary purpose of pipelining in processor design?

a) To increase clock frequency

b) To reduce power consumption

c) To improve instruction throughput

d) To decrease cache latency

Answer: c) To improve instruction throughput

Explanation: Pipelining enables simultaneous execution of multiple instructions by breaking down the execution process into smaller stages, thus improving instruction throughput and overall performance.

4. What is the main advantage of SIMD (Single Instruction, Multiple Data) processing?

a) Increased clock speed

b) Reduced power consumption

c) Enhanced parallelism

d) Improved cache hit rate

Answer: c) Enhanced parallelism

Explanation: SIMD allows a single instruction to operate on multiple data elements simultaneously, thereby exploiting parallelism and improving processing efficiency for tasks involving repetitive operations on large datasets.

5. Which level of the memory hierarchy typically has the fastest access time?

a) Main Memory

b) Cache Memory

c) Secondary Storage

d) Virtual Memory

Answer: b) Cache Memory

Explanation: Cache memory is located closest to the CPU and has the fastest access time among the memory hierarchy levels, enabling quicker retrieval of frequently accessed data.

6. What is the primary benefit of multi-core processors?

a) Increased clock frequency

b) Improved cache efficiency

c) Enhanced parallelism

d) Reduced power consumption

Answer: c) Enhanced parallelism

Explanation: Multi-core processors contain multiple CPU cores on a single chip, allowing for concurrent execution of multiple tasks and exploiting parallelism to enhance overall performance.

7. Which technique allows a single physical processor core to execute multiple software threads concurrently?

a) Vector Processing

b) Pipelining

c) Multithreading

d) Superpipelining

Answer: c) Multithreading

Explanation: Multithreading enables concurrent execution of multiple software threads on a single processor core, improving overall utilization of resources and potentially increasing performance.

8. What is a common programming approach for maximizing performance on vector processors?

a) Sequential Execution
b) Parallel Execution
c) Branch Prediction
d) Loop Vectorization

Answer: d) Loop Vectorization
Explanation: Loop vectorization involves transforming sequential loops in code into parallel loops, leveraging the capabilities of vector processors to perform operations on multiple data elements simultaneously, thus enhancing performance.

9. Which optimization technique involves analyzing and improving the performance of individual instructions in a program?

a) Scalar Profiling
b) Loop Unrolling
c) Instruction Scheduling
d) Register Allocation

Answer: a) Scalar Profiling
Explanation: Scalar profiling focuses on identifying and optimizing individual instructions or operations within a program to improve overall performance by reducing execution time or resource usage.

10. What role do compilers play in optimizing code for modern processors?

a) They enhance cache coherence

b) They automate parallelization

c) They improve clock frequency

d) They optimize instruction scheduling

Answer: b) They automate parallelization

Explanation: Compilers analyze code and automatically apply optimization techniques such as parallelization to leverage the capabilities of modern processors, improving performance without manual intervention.

11. Which optimization technique aims to reduce the number of cache misses in a program?

a) Loop Fusion

b) Loop Interchange

c) Cache Blocking

d) Loop Unrolling

Answer: c) Cache Blocking

Explanation: Cache blocking, also known as loop blocking, partitions data into smaller blocks that fit into the cache, reducing cache misses and improving cache efficiency for iterative algorithms.

12. What is the primary focus of common sense optimizations in code development?

a) Maximizing clock frequency

b) Minimizing code complexity

c) Optimizing branch prediction

d) Enhancing instruction pipelining

Answer: b) Minimizing code complexity

Explanation: Common sense optimizations aim to simplify code structure and logic, making it more readable and maintainable while potentially improving performance by reducing overhead and unnecessary computations.

13. Which optimization technique involves reordering instructions to minimize pipeline stalls and improve instruction throughput?

a) Loop Unrolling
b) Instruction Pipelining
c) Loop Fusion
d) Instruction Scheduling

Answer: d) Instruction Scheduling

Explanation: Instruction scheduling rearranges the order of instructions in a program to maximize pipeline utilization and minimize stalls, thereby improving overall execution efficiency and performance.

14. What is the primary purpose of superpipelining in processor design?

a) To increase clock frequency
b) To reduce power consumption
c) To improve instruction throughput
d) To decrease cache latency

Answer: a) To increase clock frequency

Explanation: Superpipelining breaks down instruction execution into even smaller stages than traditional pipelining, allowing for higher clock frequencies and potentially faster overall

performance.

15. Which type of processor architecture typically focuses on processing large amounts of data with a high degree of parallelism?

a) RISC
b) CISC
c) VLIW
d) SIMD

Answer: d) SIMD
Explanation: SIMD (Single Instruction, Multiple Data) architecture specializes in processing large datasets with parallel operations, making it suitable for tasks requiring extensive data manipulation, such as multimedia processing and scientific computing.

16. Which optimization technique involves combining multiple loops into a single loop to reduce loop overhead?

a) Loop Interchange
b) Loop Unrolling
c) Loop Fusion
d) Loop Blocking

Answer: c) Loop Fusion
Explanation: Loop fusion merges multiple loops that operate on the same data into a single loop, reducing loop overhead and potentially improving cache locality and performance.

17. What is the primary advantage of multi-threaded processors?

a) Increased clock frequency

b) Enhanced parallelism

c) Improved cache efficiency

d) Reduced power consumption

Answer: b) Enhanced parallelism

Explanation: Multi-threaded processors can execute multiple threads concurrently, increasing overall system throughput and efficiency by exploiting parallelism in software execution.

18. Which type of memory hierarchy level has the largest capacity but the slowest access time?

a) Cache Memory

b) Main Memory

c) Secondary Storage

d) Virtual Memory

Answer: c) Secondary Storage

Explanation: Secondary storage, such as hard drives or SSDs, has the largest capacity but the slowest access time among memory hierarchy levels, typically used for long-term storage of data and programs.

19. Which optimization technique involves duplicating loop bodies to reduce loop overhead and improve instruction-level parallelism?

a) Loop Interchange

b) Loop Unrolling

c) Loop Fusion

d) Loop Blocking

Answer: b) Loop Unrolling
Explanation: Loop unrolling replicates loop bodies multiple times to reduce loop overhead and increase instruction-level parallelism, potentially improving performance by exposing more opportunities for compiler optimizations.

20. What is the primary goal of memory hierarchy in computer architecture?

a) To increase clock frequency
b) To reduce power consumption
c) To improve memory access latency
d) To enhance cache coherence

Answer: c) To improve memory access latency
Explanation: Memory hierarchy aims to reduce memory access latency by organizing memory into different levels with varying speeds and sizes, optimizing data retrieval for faster processing and improved overall performance.

21. What optimization technique aims to minimize the number of branches in a program to improve branch prediction accuracy?

a) Loop Unrolling
b) Loop Fusion
c) Loop Jamming
d) Loop Peeling

Answer: c) Loop Jamming

Explanation: Loop jamming combines multiple loops into a single loop to reduce the number of branches and improve branch prediction accuracy, potentially enhancing performance by reducing pipeline stalls.

22. What role do compilers play in optimizing code for modern processors?

a) They automate parallelization
b) They improve cache efficiency
c) They enhance clock frequency
d) They optimize memory latency

Answer: a) They automate parallelization
Explanation: Compilers analyze code and automatically apply parallelization techniques to exploit the capabilities of modern processors, improving performance by maximizing resource utilization and concurrency.

23. Which optimization technique involves predicting the outcome of conditional branches to minimize pipeline stalls?

a) Loop Unrolling
b) Branch Prediction
c) Loop Interchange
d) Loop Fusion

Answer: b) Branch Prediction
Explanation: Branch prediction anticipates the direction of conditional branches in code execution, enabling the processor to prefetch instructions and minimize pipeline stalls caused by mispredictions, thus improving performance.

24. What is the primary focus of common sense optimizations in code development?

a) Maximizing clock frequency

b) Minimizing code complexity

c) Optimizing memory usage

d) Enhancing cache coherence

Answer: b) Minimizing code complexity

Explanation: Common sense optimizations aim to simplify code structure and logic, making it more readable and maintainable while potentially improving performance by reducing overhead and unnecessary computations.

25. Which optimization technique involves reordering loop nests to improve cache locality and reduce cache misses?

a) Loop Unrolling

b) Loop Tiling

c) Loop Fusion

d) Loop Blocking

Answer: b) Loop Tiling

Explanation: Loop tiling, also known as loop blocking, rearranges nested loops to operate on smaller data blocks that fit into cache more efficiently, reducing cache misses and improving memory access patterns.

26. What is the primary advantage of super scalar processors?

a) Enhanced cache efficiency

b) Improved branch prediction

c) Increased clock frequency

d) Concurrent execution of multiple instructions

Answer: d) Concurrent execution of multiple instructions

Explanation: Super scalar processors can execute multiple instructions simultaneously within a single clock cycle, exploiting instruction-level parallelism to enhance performance and throughput.

27. Which optimization technique involves breaking down iterations of a loop to expose parallelism?

a) Loop Jamming

b) Loop Unrolling

c) Loop Interchange

d) Loop Vectorization

Answer: d) Loop Vectorization

Explanation: Loop vectorization transforms sequential loops into parallel loops by operating on multiple data elements simultaneously, leveraging processor SIMD capabilities to improve performance through parallel execution.

28. What is the primary purpose of multi-threaded processors?

a) Increased clock frequency

b) Enhanced parallelism

c) Improved cache efficiency

d) Reduced power consumption

Answer: b) Enhanced parallelism

Explanation: Multi-threaded processors can execute multiple threads concurrently, increasing overall system throughput and efficiency by exploiting parallelism in software execution.

29. Which optimization technique involves reordering instructions to maximize pipeline utilization?

a) Instruction Scheduling

b) Loop Unrolling

c) Loop Tiling

d) Branch Prediction

Answer: a) Instruction Scheduling

Explanation: Instruction scheduling rearranges the order of instructions in a program to maximize pipeline utilization and minimize stalls, thereby improving overall execution efficiency and performance.

30. What is the primary goal of memory hierarchy in computer architecture?

a) To increase clock frequency

b) To reduce power consumption

c) To improve memory access latency

d) To enhance cache coherence

Answer: c) To improve memory access latency

Explanation: Memory hierarchy aims to reduce memory access latency by organizing memory into different levels with varying speeds and sizes, optimizing data retrieval for faster processing and improved overall performance.

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