

### Table of Contents



The basic computer has 8 registers.

The registers in the processor can be put in two categories:

- 1. User-Visible Registers:
  - 1. General purpose registers:
  - 2. Data registers:
  - 3. Address registers:
- 2. Control and Status Registers:
  - 1. Program counter (PC):
  - 2. Instruction register (IR):
  - 3. Memory address register (MAR):
  - 4. Memory buffer register (MBR):

Related posts:

- Registers are temporary storage locations inside the CPU.
- A register is a very very fast memory that is built into the CPU.
- Registers are used to store data temporarily..
- Different processors have different register.
- Registers are normally measured by the number of bits they can hold, for example, an 8-bit register means it can store 8 bits of data or a 32-bit register means it can store 32 bit of data.

The basic computer has 8 registers.

Register Symbol	Register Name	Description
AC	Accumulator	Store Result
DC	Data Register	Store Memory Data

TR	Temporary Register	Store Temporary Data
IR	Instruction Register	Store Instruction Code
AR	Address Register	Store Memory Address
PC	Program Counter	Store Address of Next Instruction
INPR	Input Register	Store Input Data
OUTR	Output Register	Store Output Data

---

The registers in the processor can be put in two categories:

1. User-visible registers
2. Control and status registers

### 1. User-Visible Registers:

Enables the machine to minimize main memory references by optimizing use of registers.

User-visible registers includes,

#### 1. General purpose registers:

General-purpose register can contain the operand for any opcode. General-purpose registers can be used for addressing functions (e.g., register indirect, displacement).

## 2. Data registers:

Data registers may be used only to hold data and cannot be employed in the calculation of an operand address.

## 3. Address registers:

Address registers may themselves be somewhat general purpose, or they may be devoted to a particular addressing mode.

Examples include the following:

- Segment pointers: Segment register holds the address of the base of the segment.
- Index registers: These are used for indexed addressing and may be autoindexed.
- Stack pointer: This allows implicit addressing; that is, push, pop, and other stack instructions need not contain an explicit stack operand.

## 2. Control and Status Registers:

Used by the control unit to control the operation of the processor.

### 1. Program counter (PC):

Contains the address of an instruction to be fetched.

### 2. Instruction register (IR):

Contains the instruction most recently fetched.

### 3. Memory address register (MAR):

Contains the address of a location in memory.

### 4. Memory buffer register (MBR):

Contains a word of data to be written to memory or the word most recently read.

#### Related posts:

1. Structure of Desktop computers
2. Logic Gates
3. Bus structure in Computer Organization
4. Addressing modes
5. Register Transfer Language
6. Numerical problem on Direct mapping
7. Registers in Assembly Language Programming
8. Array in Assembly Language Programming
9. Net 31
10. How to start with GNU Simulator 8085
11. Cache Updating Scheme
12. Cache Memory
13. Principle of Cache Memory
14. Cache Mapping
15. Addition and subtraction in fixed point numbers
16. PCI Bus
17. Booths Algorithm
18. Write a short note on design of arithmetic unit ?

19. Write a short note on Array processors ?
20. Write a short note on LRU algorithm ?
21. What is the format of Micro Instruction in Computer Architecture explain ?
22. What is the layout of pipelined instruction in Computer Architecture ?
23. Explain the following interfaces in Detail:PCI Bus, SCSI Bus, USB Bus
24. What is Memory Organization ? Discuss different types of Memory Organization in Computer System.
25. Computer Organization Q and A
26. Write short note on improving cache performance methods in detail ?
27. What is Multiprocessor ? Explain inter process communication in detail ?
28. Briefly explain the concept of pipelining in detail ?
29. Discuss the following in detail: RISC architecture, Vector processing ?
30. Define the instruction format ? Explain I/O System in detail ?
31. Explain the design of arithmetic and logic unit by taking on example ?
32. Explain how addition and subtraction are performed in fixed point number ?
33. Explain different modes of data transfer between the central computer and I/O device ?
34. Differentiate between Serial and parallel data transfer ?
35. Explain signed magnitude, signed 1's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
36. If cache access time is 100ns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?

40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
42. Explain SIMD array processor along with its architectural diagram ?
43. Write short notes on
44. Draw the functional and structural views of a computer system and explain in detail ?
45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn's taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
56. Computer Organization Previous Years Solved Questions
57. Booths algorithm to multiply +5 and -15