Ans. The arithmetic unit is a critical component of any computer system, responsible for performing arithmetic and logical operations on data.

The design of an arithmetic unit is based on the principles of digital logic circuits and computer architecture.

The arithmetic unit typically consists of several functional blocks, including adders, multipliers, and dividers, each performing a specific arithmetic or logical operation. These blocks are designed using logic gates such as AND, OR, and XOR gates, and flip-flops to store intermediate results.

The design of the arithmetic unit also involves choosing the appropriate data formats and precision levels, such as fixed-point or floating-point formats, to ensure accurate calculations. The precision level determines the number of bits used to represent the data, and higher precision usually leads to more accurate results, but at the cost of increased hardware complexity and slower performance.

The arithmetic unit is also designed to support various instruction sets, such as addition, subtraction, multiplication, and division, as well as logical operations such as AND, OR, and NOT. The unit must be able to execute these instructions in a timely and efficient manner, with minimal delays or bottlenecks.

In modern computer architectures, arithmetic units are typically implemented using integrated circuits (ICs) or specialized hardware, such as digital signal processors (DSPs) or graphics processing units (GPUs). These specialized units can perform complex arithmetic and logical operations with high speed and accuracy, making them essential for many applications, such as scientific computing, signal processing, and multimedia processing.

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21. What is the format of Micro Instruction in Computer Architecture explain ?
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26. Write short note on improving cache performance methods in detail ?
27. What is Multiprocessor ? Explain inter process communication in detail ?
28. Briefly explain the concept of pipelining in detail ?
29. Discuss the following in detail: RISC architecture, Vector processing ?
30. Define the instruction format ? Explain I/O System in detail ?
31. Explain the design of arithmetic and logic unit by taking on example ?
32. Explain how addition and subtraction are performed in fixed point number ?
33. Explain different modes of data transfer between the central computer and I/O device ?
34. Differentiate between Serial and parallel data transfer ?
35. Explain signed magnitude, signed l's complement and signed 2's complement representation of numbers. Find the range of numbers in all three representations for 8 bit register.
36. If cache access time is lOOns, main memory access time is 1000 ns and the hit ratio is 0.9. Find the average access time and also define hit ratio.
37. Explain hardwired microprogrammed control unit ? What is address sequencer circuit ?
38. Explain how a stack organized computer executes instructions? What is Stack?
39. Draw and explain the memory hierarchy in a digital computer. What are advantages of cache memory over main memory?
40. What is Associative memory? Explain the concept of address space and memory space in Virtual memory.
41. What is Paging? Explain how paging can be implemented in CPU to access virtual memory.
42. Explain SIMD array processor along with its architectural diagram ?
43. Write short notes on
44. Draw the functional and structural views of a computer system and explain in detail ?

45. Explain general register organization.
46. Compare and contrast DMA and I/O processors ?
47. Define the following: a) Flynn’s taxonomy b) Replacement algorithm
48. Explain the various pipeline vector processing methods ?
49. Describe the language features for parallelism ?
50. What are different addressing modes? Explain them.
51. Explain any page replacement algorithm with the help of example ?
52. What is mapping? Name all the types of cache mapping and explain anyone in detail.
53. Explain arithmetic pipeline ?
54. Write short notes on, a) SIMD, b) Matrix multiplication c) Instruction format
55. Differentiate: a) Maskable and non-maskable interrupt b) RISC and CISC
56. Computer Organization Previous Years Solved Questions
57. Booths algorithm to muliyiply +5 and -15